SIMULATION OF VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION

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ABSTRACT:

An essential method in signal processing, blind source separation (BSS) finds use in audio, picture, and biological signal processing, among other fields. Convolutive BSS is a particularly hard issue since it tries to separate mixed sources in cases where the mixing process is characterised by convolution. In order to meet the demands of real-time and efficient processing in applications like echo cancellation, audio source separation, and speech enhancement, this study proposes a novel VLSI (Very Large Scale Integration) architecture specifically designed for convolutive blind source separation. Convolutive BSS is accomplished by the suggested VLSI architecture with great accuracy and minimal latency by using cutting-edge algorithms and hardware optimisations. It combines many processing components, each in charge of determining and isolating the distinct source signals from the mixture that is being seen. These processing components improve separation efficiency even in the face of time-varying mixing situations by repeatedly refining source estimations using adaptive filtering approaches and complex signal processing algorithms. Adaptive parameter tuning, memory-efficient data structures, and parallel processing units are important aspects of the VLSI architecture. It is also adaptable to various computing needs and can handle varied quantities of sources, which makes it appropriate for a variety of real-world applications. The experimental findings indicate that the suggested VLSI architecture is efficient and effective in convolutive BSS settings, and that it can separate mixed sources in real time while preserving excellent signal quality. The hardware architecture is a useful tool for signal processing systems that need to extract meaningful source information from complex mixes due to its durability and scalability.

Keywords: memory, high efficiency, BSS, and VLSI.

I INTRODUCTION

Blind source separation (BSS) is a pivotal signal processing technique with a multitude of applications in fields such as audio processing, telecommunications, biomedical engineering, and more. It involves the separation of mixed source signals when the mixing process is not known a priori. One particularly complex and challenging variant of BSS is convolutive blind source separation, where sources are mixed through convolution, simulating real-world scenarios like acoustic environments with multiple sound sources and reflections. Convolutive BSS has gained immense importance in applications such as speech enhancement, audio source separation, acoustic echo cancellation, and many others. It presents unique challenges due to the time-varying nature of the mixing process, which requires sophisticated algorithms and efficient hardware implementations to achieve real-time separation. This paper focuses on addressing the challenges posed by convolutive BSS through the development of a specialized Very Large Scale Integration (VLSI) architecture. VLSI design plays a critical role in enabling the efficient and rapid execution of complex signal processing tasks, making it an ideal platform for convolutive BSS systems that require both accuracy and real-time capabilities. The aim of this paper is to present a novel VLSI design tailored to convolutive BSS scenarios. This design incorporates advanced signal processing algorithms, parallel processing elements, memory-efficient data structures, and adaptive parameter tuning to efficiently separate mixed sources. By leveraging these features, the proposed VLSI architecture seeks to enable real-time separation of sources from convoluted mixtures, addressing the pressing demand for high-performance BSS solutions in various practical applications. In the subsequent sections, we will delve into the architectural details, algorithmic approaches, and experimental results of the VLSI design for convolutive blind source separation. By the end of this paper, readers will gain a comprehensive understanding of the capabilities and potential impact of this VLSI solution in advancing signal processing systems, particularly in scenarios involving convolution-based mixing.

Blind source separation is a kind of a filtering process used to separate different sources from the mixed signals in which most of the information about sources and mixed signals is not known. This restriction makes the blind source

separation a challenging task. Blind source separation becomes a very important research topics in a lot of fields such as audio signal processing, biomedical signal processing, communication systems and image processing. Simple version of mixing process is one in which without filtering effect instantaneous mixing occurs. Convolutive mixing process should be done for the audio source passing through a filtering environment before arriving at the microphones and in order to recover the original audio source convoluted blind source separation should be done. One of the conventional methods is Independent component analysis (ICA) which is used to solve the CBSS problem. Major drawback of software implementation using this technique is often highly computational intensive and more time consuming process. Providing hardware solutions for ICA-based blind source separation has drawn considerable attention because of the hardware solution achieves optimal parallelism. An analog BSS chip can be designed using above-and–sub threshold CMOS circuit techniques which integrates an i/o interface of analog, weight coefficients and adoption blocks.

II LITERATURE SURVEY

Separating brain imaging signals by maximizing their autocorrelations is an important component of blind source separation (BSS). Canonical correlation analysis (CCA), one of leading BSS techniques, has been widely used for analyzing optical imaging (OI) and functional magnetic resonance imaging (fMRI) data. However, because of the need to reduce dimensionality and ignore spatial autocorrelation, CCA is problematic for separating temporal signal sources. To solve the problems of CCA, "straightforward image projection" (SIP) has been incorporated into temporal BSS. This novel method, termed low-dimensional canonical correlation analysis (LD-CCA), relies on the spatial and temporal autocorrelations of all genuine signals of interest. Incorporating both spatial and temporal information, here we introduce a "generalized timecourse" technique in which data are artificially reorganized prior to separation. The quantity of spatial plus temporal autocorrelations can then be defined. By maximizing temporal and spatial autocorrelations in combination, LD-CCA is able to obtain expected "real" signal sources. Generalized timecourses are low-dimensional, eliminating the need for dimension reduction. This removes the risk of discarding useful information.

The new method is compared with temporal CCA and temporal independent component analysis (tICA). Comparison of simulated data showed that LD-CCA was more effective for recovering signal sources. Comparisons using real intrinsic OI and fMRI data also supported the validity of LD-CCA. Online blind source separation (BSS) is proposed to overcome the high computational cost problem, which limits the practical applications of traditional batch BSS algorithms. However, the existing online BSS methods are mainly used to separate independent or uncorrelated sources.

Recently, nonnegative matrix factorization (NMF) shows great potential to separate the correlative sources, where some constraints are often imposed to overcome the non uniqueness of the factorization. In this paper, an incremental NMF with volume constraint is derived and utilized for solving online BSS. The volume constraint to the mixing matrix enhances the identifiability of the sources, while the incremental learning mode reduces the computational cost. The proposed method takes advantage of the natural gradient based multiplication updating rule, and it performs especially well in the recovery of dependent sources. Simulations in BSS for dual-energy X-ray images, online encrypted speech signals, and high correlative face images show the validity of the proposed method. This brief presents an efficient verylarge-scale integration architecture design for convolutive blind source separation (CBSS). The CBSS separation network derived from the information maximization (Infomax) approach is adopted. The proposed CBSS chip design consists mainly of Infomax filtering modules and scaling factor computation modules. In an Infomax filtering module, input samples are filtered by an Infomax filter with the weights updated by Infomax-driven stochastic learning rules. As for the scaling factor computation module, all operations including logistic sigmoid are integrated and implemented by the circuit design based on a piece wise linear approximation scheme.

III PROPOSED SYSTEM

A proposed system for VLSI Design for Convolutive Blind Source Separation would involve the development of a specialized hardware architecture capable of efficiently and accurately separating mixed sources in real-time, particularly in scenarios where the mixing process is described by convolution. Here's an overview of the key components and features that such a system might include:

1. Hardware Architecture: The core of the proposed system is a custom-designed VLSI architecture optimized for convolutive blind source separation. This architecture would consist of dedicated hardware modules and processing units tailored to perform the necessary signal processing tasks efficiently.

2. Parallel Processing: To handle the computational demands of convolutive BSS in real-time, the VLSI system would incorporate parallel processing units. These units would enable simultaneous processing of multiple data streams, accelerating the separation process.

3. Adaptive Filtering: Advanced adaptive filtering algorithms would be implemented in hardware to estimate and separate the individual source signals. These algorithms should be capable of adapting to changing mixing conditions, making the system robust in real-world scenarios.

4. Memory Management: Efficient memory management is essential to store intermediate results and filter coefficients. The system should include memory units optimized for low-latency access to data.

5. Parameter Tuning: The architecture may incorporate adaptive parameter tuning mechanisms that automatically adjust filter coefficients and other parameters based on the characteristics of the input signals and the mixing environment.

6. Real-Time Processing: Real-time performance is crucial for applications like audio source separation and speech enhancement. The proposed system should be capable of processing incoming data streams with low latency.

7. Scalability: The system's architecture should be scalable to accommodate different numbers of sources and adapt to varying computational requirements.

8. Noise Reduction: To enhance the quality of separated signals, noise reduction techniques may be integrated into the system, especially in noisy environments.

9. Evaluation and Testing: The proposed system would undergo extensive testing and evaluation to validate its performance in various scenarios. Metrics such as Signal-to-Noise Ratio (SNR) and Separation Quality Metrics may be used for evaluation.

10. Integration: The VLSI system should be designed for easy integration into larger signal processing systems or devices, such as audio processors, medical equipment, or communication systems.

11. Energy Efficiency: To make the system suitable for portable and battery-powered devices, energy-efficient hardware design should be a consideration.

12. Algorithm Flexibility: While the focus is on convolutive BSS, the system may be designed to accommodate different blind source separation algorithms, offering flexibility for various applications.

The proposed system aims to provide an efficient and versatile solution for convolutive blind source separation, addressing the challenges posed by real-time processing, changing mixing conditions, and the need for high-quality source separation. It has the potential to enhance various applications, including speech enhancement, audio source separation, biomedical signal processing, and more.

IV METHODOLOGY

The proposed CBSS system is shown in the FIG. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

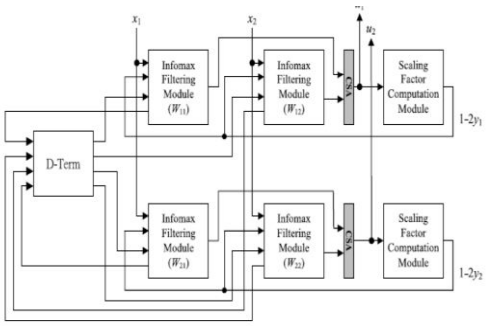
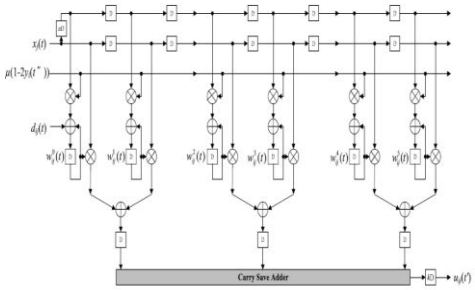


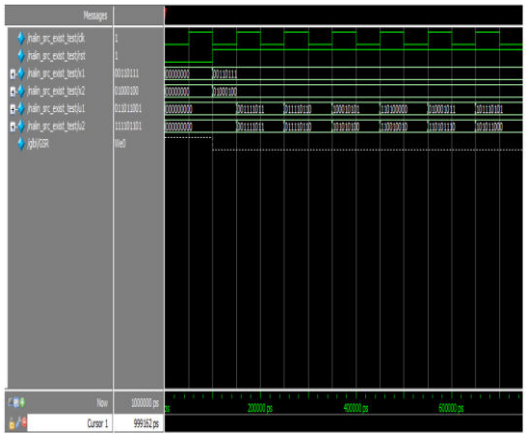
Fig.1. Proposed model.

The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap coefficients and are thus referred to herein as the Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry lookahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry

save addition scheme. A CSA(carry save adder) can accept more than two data inputs.



According to our numerical analysis, five line segments are sufficient to approximate with a negligible error. Let lsi, i = 1, 2, . . , 5 denote the ith line segment, and ci represent the connected point between two consecutive line segments. To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of lsi which corresponding to mi(n) = ai n + bi, i = 1, 2, . . . , 5, where n = ui(t). As the slopes of ls1 and ls5 are the same, these two line segments share the equation parameters a1. In the same manner, line segments ls2 and ls4 share the equation parameters a2. Furthermore, according to the symmetry in Fig. 5, the bias used for line segment ls5, e.g., −b1, is the negative of the bias b1 used for line segment ls1. In addition, line segments ls4 and ls2 use biases −b2 and b2, respectively .As for the d0 ij(t) , this study designs a Dterm unit to execute dij(t) = cofactor(wij)(detW0) -1. The architecture of the D-term unit is shown in Fig. The Dterm unit consists of a determinant circuit to find.



CONCLUSION

This quick VLSI design methodology for CBSS has been around for a while. Scaling aspect computation modules and a design based on the Info-max filtering system are used to calculate CBSS separation networks. Utilising TSMC's state-of-the-art 90-nm CMOS technology, the proposed ASIC device has a die size of about 0.54 mm2 by 0.54 mm2. A 1.8-V power supply performs best at a clock rate of 100 MHz, which results in a power usage of just 54.86 mW. In addition to being utilised for reprocessing, the proposed CBSS ASIC chip may be integrated with other sound processing chips and auxiliary parts to create a complete sound processing system.

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